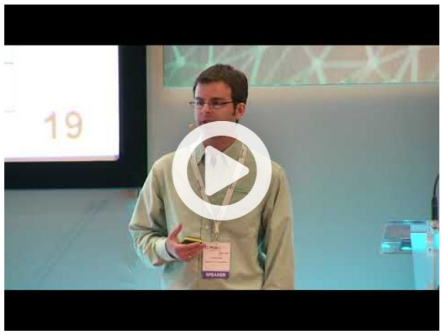
# EXHIBIT E

BLOG

May 24th, 2018



# Securing High-performance RISC-V Processors from Time Speculation @ RISC-V Barcelona Workshop

Christopher Celio and Jose Renau, CPU Architects from Esperanto Technologies, discussed potential changes to future high-performance RISC-V processors intended to eliminate speculation-based timing attacks, such as Spectre and Meltdown. They presented a proposal for RISC-V cores which minimizes changes to the RISC-V ISA or platform specifications in order to provide security against timing-based attacks.

**Admission is free:**

Admission is free to qualified registrants. The conference is intended for chip designers, system designers, equipment vendors, OEM/ODMs, service providers, press, and the financial community. Esperanto is a Gold sponsor of the Linley Fall Processor Conference.

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